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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
MP0798

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

On July 26, 2007

Signature Diane M. Schmidt

Typed or printed name Diane M. Schmidt

Application Number 10/686,151	Filed October 15, 2003
First Named Inventor Dinesh Jayabharathi et al.	
Art Unit 2138	Examiner Dipakkumar B. Gandhi

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

NOTICE OF APPEAL IS ATTACHED (in duplicate).

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

PRE-APPEAL BRIEF REQUEST FOR REVIEW IS ATTACHED (5 pages).

I am the

☐ applicant/inventor

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 34,754.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

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July 26, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/686,151

Filing Date: October 15, 2003

Applicant: Dinesh Jayabharathi et al.

Group Art Unit: 2138

Examiner: Dipakkumar B. Gandhi

Title: SYSTEM AND METHOD FOR USING TAP CONTROLLERS

Attorney Docket: MP0798

Mail Stop AF
Commissioner for Patents
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Alexandria, Virginia 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants request a Pre-Appeal Brief Conference and contend that there is no suggestion or motivation to modify the teachings of Henson et al. (European Pat. No. 0622726 A2) with the teachings of Szczepanek et al. (U.S. Pub. No. 2003/0110344), and further that the combination of Henson and Szczepanek fails to teach or suggest the elements of the presently pending claims.

STATUS OF CLAIMS

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Henson et al. (European Pat. No. 0622726 A2) in view of

Szczepanek et al. (U.S. Pub. No. 2003/0110344). Claims 14-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable Henson et al. (European Pat. No. 0622726 A2) in view of Szczepanek et al. (U.S. Pub. No. 2003/0110344) and Noguchi (U.S. Pub. No. 2002/00626466 A1).

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 14 recites a method for accessing internal memory of a disk controller. Disk controller control data is stored on a first memory that is located on the disk controller and transferred to a second memory located on a test access port (TAP) controller. The TAP controller is located on the disk controller. In other words, the **disk controller control data is transferred to the second memory located on the TAP controller, which is itself located on the disk controller**. Independent claims 22 and 29 recite similar subject matter.

Independent claim 1 recites a method for dynamically writing to an internal register space of a chip **using a test access port (TAP) controller**. Specifically, the method includes gaining access to the internal register space **during normal operation of the chip**. Independent claims 4, 7, 12 recite similar subject matter. For example, claim 4 recites a method that includes gaining access to the internal register space during normal operation of the chip and transferring information to a register in the TAP controller.

ARGUMENT

Applicants submit that there is no suggestion or motivation to combine the teachings of Henson with Szczepanek, and that such a combination, even if appropriate, fails to teach or suggest at least i) that disk controller control data is transferred to a second memory on a TAP controller that is located on a disk controller; and/or ii) gaining access to the internal register space during normal operation of a chip.

Initially, Applicants note that the alleged combination of Henson with Szczepanek and/or Noguchi is improper and the Examiner has failed to support his alleged motivation to combine these references using actual evidence as required. (Pages 10-13 of the Response filed February 8, 2007, hereinafter "the Response).

Henson, which describes **hard disk drive (HDD) architecture**, lacks any teaching or suggestion of a test access port (TAP) and a TAP controller. The Examiner acknowledges this deficiency and instead relies on Szczepanek to disclose a TAP and a TAP controller. Szczepanek is not directed to HDDs and/or HDD controllers and is absent of any teaching or suggestion of such a structure. Instead, Szczepanek is directed to **a communications system**. In other words, Henson is directed to HDD architecture and lacks any teaching or suggestion of a TAP controller, and Szczepanek is directed to a communications system that includes a JTAG interface.

One skilled in the art presented with Henson, which is directed to **HDD architecture** and is absent of any teaching or suggestion of a TAP controller, would not be motivated to look to Szczepanek, which is directed to **a communications system** that includes a JTAG interface. Szczepanek is absent of any teaching or suggestion of storage disks, disk controllers, and/or access of storage disk control data. In view of the above, Applicants respectfully assert that the Examiner has failed to clearly and particularly support his alleged motivation to combine these references using actual evidence as required.

With respect to claim 14, Applicants further note that even if proper, the combination still fails to disclose transferring **disk controller control data** from a first memory on a disk controller to **a second memory located on a test access port controller**. Instead, Szczepanek appears to disclose transferring JTAG test instructions to the alleged second memory. (Pages 13-14 of the Response).

Applicants note that the Examiner **initially acknowledged that Henson does not disclose this limitation** (Page 5, Lines 20-22 of the Office Action mailed October 13, 2006) and instead relied on Page 29, Paragraphs [0408]-[0416] of Szczepanek to disclose disk controller control data. Applicants noted that these cited portions of Szczepanek merely disclose transferring JTAG instructions, not **storage controller control data**. The Examiner now alleges that Henson discloses this limitation at Column 3, Lines 17-22 and teaches that **the second memory is located on a TAP controller**. (Page 3, Lines 18-22 of the present Office Action). As previously mentioned, the Examiner **acknowledges that Henson does not disclose a TAP controller**. As such, Applicants fail to comprehend how Henson can disclose that the second memory is located on the TAP controller when Henson is absent of any teaching or suggestion of the TAP controller.

Applicants further note that claim 1 recites a method for dynamically writing to an internal register space of a chip using a TAP controller **without interfering with normal operation of the chip**. (Pages 14-15 of the Response). In contrast, Szczepanek discloses accessing RAM **during testing**. (See Paragraph [0416]). As described in Applicants' specification, typically all chip operations stop during JTAG testing. (See Paragraph [0008] of the present application). Szczepanek appears to be absent of any teaching or suggestion of allowing access to internal register space during normal chip operation as claim 1 recites.

Applicants respectfully submit that there is no suggestion or motivation to modify the HDD controller of Henson with the teachings of Szczepanek. Even if proper, Applicants further submit that such a combination fails to teach or suggest one or more limitations of the claims. Accordingly, Applicants respectfully submit that the presently pending claims are in condition for allowance.

Respectfully submitted,

Dated: July 26, 2007

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